2007 IEEE Device Research Conference: *Tour de Force* Multigate and Nanowire Metal Oxide Semiconductor Field-Effect Transistors and Their Application

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ABSTRACT Scaling of the conventional planar complementary metal oxide semiconductor (CMOS) faces many challenges. Top-down fabricated gate-all-around Si nanowire FinFETs, which are compatible with the CMOS processes, offer an opportunity to circumvent these limitations to boost the device scalability and performance. Beyond applications in CMOS technology, the thus fabricated Si nanowire arrays can be explored as biosensors, providing a possible route to multiplexed label-free electronic chips for molecular diagnostics.

New materials and device structures are required to allow metal oxide semiconductor field-effect transistor (MOSFET) channel length scaling to the sub-10 nm regime. Si nanowires, using either bottom-up or top-down fabrication approaches, are promising components for ultrashort channel devices. Bottom-up Si nanowires are typically grown by the vapor–liquid–solid (VLS) method using a Au catalyst and are integrated into device structures by special assembly techniques. This bottom-up approach can result in atomically smooth semiconductor structures; however, Au contamination poses a significant challenge. Recently, Si nanowire MOSFETs have been successfully fabricated using a top-down approach, which may be more compatible with conventional MOSFET fabrication and complementary metal oxide semiconductor (CMOS) processes. At the IEEE Device Research Conference (DRC) in South Bend, Indiana, in June 2007, Balasubramanian and colleagues presented structural, material, and device performance results for Si nanowire MOSFETs fabricated using a top-down approach.[1] Si nanowire arrays have also been applied in biosensors and may provide a new route to integrate biotechnology with CMOS technology.

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Advantages of FinFETs for CMOS Scalability. Scaling of the traditional planar CMOS is limited by a number of issues, including mobility degradation, channel doping fluctuation, and, most importantly, charge control and short channel effects. For very short channel lengths, it is difficult to maintain the two-dimensional character of longer channel devices, and, increasingly, the electric field from the drain electrode influences or controls channel charge and conduction (drain-induced barrier lowering, DIBL). This difficulty, together with reduced operating voltages for scaled constant-field MOSFETs and the unscaled thermal-voltage-related subthreshold dependence of drain current on gate voltage, results in device threshold voltages that shift with gate length and drain voltage, increased subthreshold slope, and increased and unacceptable device leakage in the off state. Scaling gate dielectric thickness has historically been a key tool for scaled MOSFETs, but currently, dielectric thickness is limited to about 1.2 nm by tunneling (which leads to unacceptable leakage current). Additionally, high-*k* dielectrics offer only modest advantages.

Dual- and multiple-gate MOSFETs can provide improved channel charge control for short channel lengths as compared to conventional single-gate planar MOSFETs, at the cost of increased fabrication complexity.[2] FinFETs, nanowire, and other three-dimensional (3D) MOSFETs are being actively researched as candidate replacements for planar MOSFETs in ultrashort channel length devices.

FinFETs use a narrow (a few tens of nanometers or less) Si fin with gates (with lengths also a few tens of nanometers or

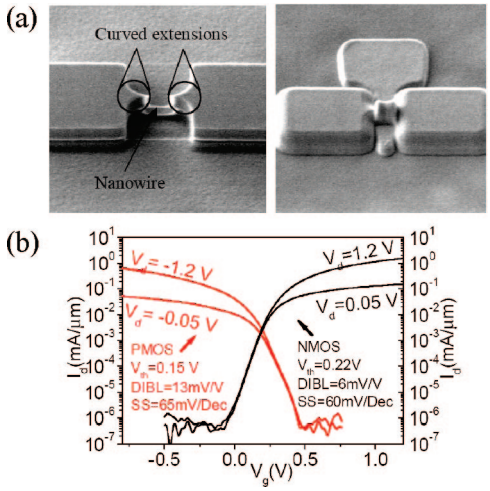

Figure 1. (a) Top view SEM images of the released 200 nm long and 3 nm wide Si nanowire before (left) and after (right) gate definition. (b) I_d *vs* V_g plot with current normalized to nanowire radius. Excellent short channel performance is observed. Adapted from ref 4.

less) on the vertical sides or sides and top. The multiple gates, together with the thin device body, dramatically enhance gate control of the channel charge and reduce short channel effects compared to conventional planar devices. In addition, because channel doping is typically not used for channel confinement or threshold voltage control in FinFETs, channel mobility can be enhanced, and device variations from statistical doping fluctuations can be reduced. The device structure also lends itself readily to strain-enhanced transport.

Top-Down Fabricated Gate-All-Around Si Nanowire FinFETs. In 1999, Hu and coworkers at the University of California, Berkeley, fabricated double-gate FinFETs on silicon-on-insulator (SOI) substrates.[3] Recently, Balasubramanian and colleagues from the Institute of Microelectronics in Singapore and Yeo and co-workers from Samsung Electronics Co. have separately demonstrated gate-all-around (GAA) Si nanowire MOSFETs.[1,4,5] In these demonstrations, Si nanowires were fabricated using a top-down approach on either thin-body SOI or bulk Si substrates. Balasubramanian *et al.* employed alternating phase shift mask lithography and a deep UV source to pattern Si fins of 40–50 nm width on thin SOI. Dry thermal oxidation, a self-limiting process, was then used to shrink the dimensions of the fin down to 3–6 nm, leading to the formation of two Si nanowires wrapped by thermal oxide.[4] After the top Si nanowire was selectively etched away and the bottom one released from buried oxide, the gate oxide and polysilicon gate were deposited all around the suspended Si nanowire, as illustrated in Figure 1a. The GAA Si nanowire MOSFET displays high current drive, nearly ideal subthreshold swing, and low DIBL, all evidence of excellent short channel performance, as shown in Figure 1b. Yeo *et al.* used a SiGe sacrificial layer and a SiN hard mask to fabricate twin GAA Si MOSFETs with 4 nm nanowire radius and 15 nm length TiN metal gates on bulk Si substrates.[5] Despite the short gate length, excellent short channel performance was demonstrated. The authors also presented evidence of quasi-ballistic room temperature transport, indicating that their semiconductor nanowires are high quality.

Threshold voltage control by channel doping is not practical for FinFETs because of the small channel dimensions. Instead, the principal mechanism for threshold voltage control is the gate work function. Metal gates with work functions located in the semiconductor bandgap are required, and the metal must also be compatible with the thermal processing required for device fabrication. Liu *et al.* from the National Institute of Advanced Industrial Science and Technology in Japan compared TiN and polysilicon gate FinFETs, and they demonstrated that TiN can result in larger gate capacitance and increased current drive by eliminating the carrier depletion of the semiconductor gate.[6] TiN has also been used to strain-engineer Si FinFETs to improve carrier mobility.[1,7] The work function of TiN was also shown to be adjustable by film thickness and composition, allowing a degree of threshold voltage tunability. For example, surface oxidation of a thin TiN gate led to a Ti-rich film and a lower metal work function. Both *n*- and *p*-channel devices were demonstrated (necessary for CMOS circuits) with 3 nm thick TiN used for *n*-channel devices and 20 nm thick TiN used for *p*-channel devices.[7]

Si Nanowire FinFETs with Multiple Channels. Although the thin Si region in a FinFET helps to improve short channel effects, increasing the current drive will require connecting multiple fins to the source and drain regions and controlling them by using a common gate. When multiple fins are patterned by optical lithography, the distance between fins, and therefore the current density, will be limited by the achievable pitch. At the

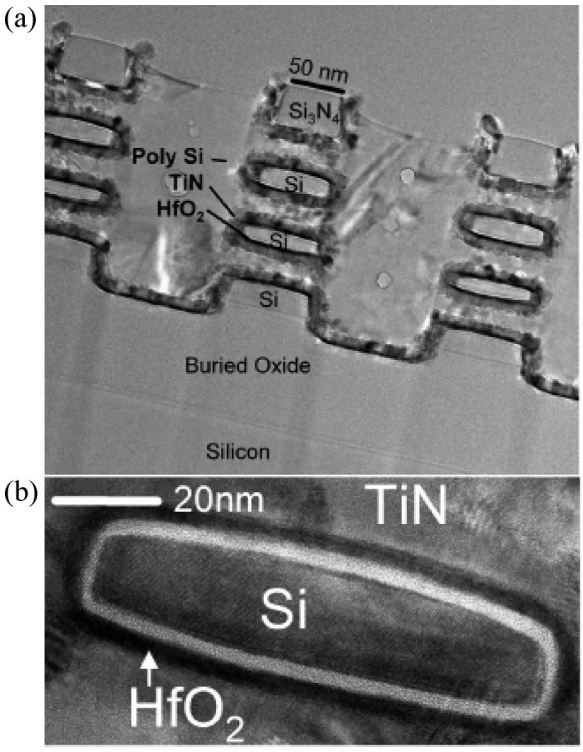

Figure 2. (a) Cross-section TEM image of the 3D stacks GAA Si nanobeam FinFET structure fabricated from SiGe/Si superlattices on SOI substrate. (b) High-resolution TEM image of the Si nanobeam surrounded by HfO_2 gate dielectric and TiN metal gate. Adapted from ref 9.

most recent IEEE International Electron Device Meeting (2006 IEDM), devices fabricated from SiGe/Si superlattices were presented as a high-density alternative.[8,9] Superlattices of SiGe/Si were grown using chemical vapor deposition (CVD) on top of a SOI substrate with the thickness of the SiGe and Si layers well controlled by epitaxial growth. Lithography and reactive ion etching were then used to define the fin structure, after which the SiGe layers were selectively removed using either thermal oxidation or dry etching (based on the differential oxidation and etching rates between SiGe and Si). This created multiple suspended and vertically stacked nanowires.[8,9] Figure 2 shows transmission electron microscopy (TEM) images of 3D stacks of GAA FinFETs with HfO_2/TiN gates fabricated from the superlattices. The 3D stacked FinFET devices demonstrated high current drive and I_{on}/I_{off} ratio and good subthreshold slope.

Rooyackers *et al.* demonstrated that fin density can be doubled or quadrupled using spacer-defined fin patterning to mitigate the lithographic pitch limitation.[10] This approach begins with a thin-body SOI. A SiGe sacrificial layer was deposited by CVD and patterned into blocks by photolithography. To double the fin density, SiN spacers formed at the sidewalls of the SiGe blocks were used as hard masks to etch Si fins after selective removal of the sacrificial SiGe. This approach can be extended to quadruple the fin density using tetraethoxysilane (TEOS) oxide sidewall spacers formed on the SiN regions as an etching mask after removal of the SiN.

Heterogeneous collections of devices containing completely different semiconductor materials and layer structures can reside side-by-side on a single substrate.

Beyond CMOS: Si Nanowire Array-Based Biosensors. In addition to using Si nanowires in FinFETs as candidates for scaled CMOS, Balasubramanian *et al.* derivatized the surfaces of oxidized Si nanowires with probe biomolecules of peptide nucleic acid to produce highly sensitive label-free biosensor arrays.[1,11] Here, they take advantage of the large surface-to-volume ratio of the nanowires, and hence the high sensitivity of channel conductance to small changes in surface charge with biomolecule binding. An important aspect of this top-down approach is the ability to integrate individually addressable Si nanowire biosensors with excellent device-to-device uniformity. This gives the potential to fabricate chips with large sensor redundancy and further improvements in detection signal-to-noise ratio and sensitivity. When combined with CMOS multiplexing, this route provides a scalable and manufacturable approach to achieving highly sensitive real-time chip-based biosensor arrays.

Top-Down or Bottom-Up? Exciting opportunities are also emerging for bottom-up semiconductor nanowire growth using VLS, and for their integration into 3D electronic and optoelectronic circuits as well as biosensor arrays. Using VLS, it is possible to grow single-crystal group IV, III-V, and II-VI semiconductor nanowires on lattice mismatched (and even amorphous) substrates. Thus, heterogeneous collections of devices containing completely different semiconductor materials and layer structures can reside side-by-side on a single substrate. Further complex axial and radial heterojunctions that would be difficult to achieve using top-down methods can be readily fabricated by combining VLS (axial) with thin-film overgrowth (radial). Considerable effort is being devoted to answering fundamental questions in VLS growth mechanisms, dopant introduction, impurity incorporation (*e.g.*, from the Au catalysts), junction abruptness, surface passivation, *etc.*, which all must be understood and controlled to realize a scalable and robust bottom-up nanowire device technology.

At the 2007 DRC, Bakkers *et al.* from Philips Research Laboratories presented vertical III-V nanowire electronics built on Si substrates.[12] The epitaxial growth challenges, including lattice mismatch and the differences in thermal expansion coefficients, are suppressed by reducing the contact area between the III-V materials and Si substrate and by making vertial structures. The integration of III-V materials with existing Si technologies would have significant impact on future integrated optoelectronic devices and circuits. IBM Zurich announced a vertical impact ionization Si nanowire FET fabricated by epitaxial growth, with greatly reduced subthreshold swing and leakage current.[13]

The ability to synthesize large quantities of different types of nanowires off-chip and then integrate them with fully processed CMOS circuits can offer even more flexibility than direct growth in place for certain types of heterogeneous integrated circuits (for example, derivatizing the surfaces of batches of nanowires with different biomolecule capture probes *en masse* under optimized conditions prior to integration). This is because diverse and incompatible chemistries can be applied prior to hierarchical assembly. This may enable high-density multianalyte biosensor arrays with performance advantages. However, the outstanding scientific and technological challenges are significant. For example, scalable and manufacturable nanowire directed assembly techniques must be developed, and defect-tolerant circuits that can accommodate inevitable variations in device nonuniformity and defects must be designed. All in all, recent advances in both top-down and bottom-up approaches illustrate the enormous potential for nanowire-based electronics.

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